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DILLON & YUDELL LLP
8911 NORTH CAPITAL OF TEXAS HWY
SUITE 2110
AUSTIN, TX 78759

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,052	ARIMILLI ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 7/27/2005.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. The examiner asserts that errors may exist within the specification.

For instance, on page 15, line 1, replace "compete" with --complete--.

Claim Objections

4. Claim 1 is objected to because of the following informalities: In the second to last line, replace "provides" with --provide--. Appropriate correction is required.

5. Claim 12 is objected to because of the following informalities: In lines 9-10, replace "advance operation" with --advanced operational--. Appropriate correction is required.

6. Claim 20 is objected to because of the following informalities: In line 5, replace "utilizes" with --utilize--. Appropriate correction is required.

Maintained Claim Rejections

7. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 10-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 10 recites the limitation "said interconnection means" in the last paragraph. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 12 recites the limitation "the SMP" in line 13 and the limitation "said second, heterogenous processor" in lines 17-18. There is insufficient antecedent basis for these limitations in the claim.

12. Claims 11 and 13-20 are rejected under 112, 2nd paragraph, for dependent upon a claim which is rejected under 112, 2nd paragraph.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory, U.S. Patent No. 6,513,057 (as applied in the previous Office Action and herein referred to as McCrory) in view of Derrick et al., U.S. Patent No. 5,704,058 (as applied in the previous Office Action and herein referred to as Derrick), and further in view of Cochcroft, Jr. et al., U.S. Patent No. 5,317,738 (herein referred to as Cochcroft).

15. Referring to claim 12, McCrory has taught has taught a multiprocessor system comprising:

a) a plurality of heterogenous processors with different operational characteristics and physical topology connected on a system planar. See the abstract, Fig.3, and column 5, line 66, to column 6, line 8.

b) a system bus that supports system centric operations. See Fig.3 and column 2, lines 36-67.

c) interrupt pins coupled to said system bus that provide connection for at least one of said plurality of heterogenous processors. See column 2, lines 40-47, and note that processors are coupled through an interface (interrupt pins) to the rest of the system.

d) an enhanced system bus protocol that supports downward compatibility of a newer processor that is designed with advanced operational characteristics from among said plurality of heterogenous processors to a first processor that does not support said advanced operational characteristics. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486. Clearly, the 80486 does not include some of the advance characteristics of the Pentium which make it compatible with the

80486 because it is in fact an 80486, and therefore it does not need to be backward compatible with an 80486.

e) McCrory has not taught an enhanced operating system (OS) that supports inter-processing operations between said first processor and said newer processor including cache coherency operations based on a collective memory configuration of the SMP. However, Derrick has taught the concept of employing cache coherency in a multiprocessor system. See column 1, lines 15-27. Cache coherency is employed so that all caches contain consistent, up-to-date data. Otherwise, if a particular cache did not have the most up-to-date data, the processor accessing that cache would be performing operations using incorrect data, which would cause delays in execution. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS to include support for cache coherency.

f) McCrory has not taught that said OS logs operating characteristics and cache topology data of each processor connected to the system bus to calculate a most efficient work allocation among processors. However Cochcroft has taught a system in which process identification codes (operating characteristics) are logged and the number of cache lines used by each process in each processor (cache topology data) is logged. This data allows for efficient allocation of workload to the processors. See column 1, lines 6-9. As a result, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS log the aforementioned data.

g) McCrory has further taught that said enhanced system bus protocol and said enhanced operating system support backward compatibility between said second, heterogenous processor and said first processor. See column 6, lines 26-33 and note that Pentiums and 80486s may be

used in the system. Pentium chips are backward compatible with 80486. In addition, the system clearly supports forward compatibility because the system can still employ SMP even though a newer family (Pentium) is used with an older family (80486).

h) McCrory has not taught providing system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states. However, Official Notice is taken that prefetching is well known and accepted in the art. Prefetching allows for fetching of instructions/data before the instructions/data are actually needed. Therefore, at the time when they are needed, they are already fetched and present in the system, thereby avoiding any waiting time that might be incurred due to fetching instructions/data as they are needed. In addition, Derrick has taught cache intervention in a multiprocessor system. See column 5, lines 4-14, and note that any L2 cache may intervene and provide the requested data. As is known, cache intervention allows an updated cache to provide data to a requesting device whose cache is not updated. This also prevents the requesting device from having to spend many cycles accessing main memory for the data. Finally, Derrick has taught an intelligent cache state enhancement. See the abstract and column 3, lines 7-17 and note the implementation of an arbitration scheme for snoop activity. Such a scheme allows for optimized performance and efficient allocation of bandwidth. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to include cache intervention and a cache arbitration scheme which optimize system performance.

16. Referring to claim 14, McCrory in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 12. Although McCrory in view of Derrick and further in view of Cochcroft has taught that said plurality of heterogenous processors

includes different numbers of processors on a single processor chip (see Fig.4), they have not explicitly taught that said plurality of processors includes heterogenous processor topologies including different cache sizes, cache states, and number of cache levels. However, McCrory has taught using heterogenous processors from different families together in a SMP system. See column 2, lines 27-47, and the abstract. And, Official Notice is taken that different processors exhibit different characteristics such as the ones listed above. Since, certain families of processors would be picked by the designer for executing different types of applications, the characteristics that ultimately exist are based on designer choice. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to include heterogeneous processors that include different cache sizes, cache states, and cache levels among the different processors because processors differ in these areas, and different processors may be selected by the designer.

17. Claims 1-7, 9-11, 13, 15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory, in view of Derrick in view of Cochcroft, as applied above, and further in view of Bacot et al., U.S. Patent No. 5,235,687 (herein referred to as Bacot).

18. Referring to claim 1, McCrory has taught a data processing system comprising:

a) a first processor with first operational characteristics on a system planar. See Fig.3, the abstract, column 2, lines 37-47, and column 5, line 66, to column 6, line 8.

b) interconnection means for connecting a second, heterogenous processor on said system planar, wherein said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system. See Fig.3, the

abstract, column 2, lines 37-47, and column 5, line 66, to column 6, line 8. McCrory has not explicitly taught later connecting a second, heterogenous processor on said system planar, wherein said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system. However, Bacot has taught a multiprocessor system in which, when an individual processor breaks or becomes defective, that individual processor is replaced so that the system can return to operating at full capacity. See column 1, lines 57-68. A person of ordinary skill in the art would have recognized that if a processor breaks in McCrory, then the broken processor could be replaced with a functioning processor, thereby allowing symmetric multiprocessing. As a result, in case of individual processor breakage, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory such that a second, heterogenous processor is later added in to the system via interconnection means to allow the system to perform at a higher level.

c) McCrory has not taught an enhanced operating system (OS) that supports inter-processing operations between said first processor and said second processor including cache coherency operations based on a collective memory configuration of the SMP. However, Derrick has taught the concept of employing cache coherency in a multiprocessor system. See column 1, lines 15-27. Cache coherency is employed so that all caches contain consistent up-to-date data. Otherwise, if a particular cache did not have the most up-to-date data, the processor accessing that cache would be performing operations using incorrect data, which would cause delays in execution. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS to include support for cache coherency.

d) McCrory has not taught that said OS logs operating characteristics and cache topology data of each processor connected to the interconnection means to calculate a most efficient work allocation among processors. However Cochcroft has taught a system in which process identification codes (operating characteristics) are logged and the number of cache lines used by each process in each processor (cache topology data) is logged. This data allows for efficient allocation of workload to the processors. See column 1, lines 6-9. As a result, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS log the aforementioned data.

e) McCrory has further taught said interconnection means and said enhanced operating system support backward compatibility between said second, heterogenous processor and said first processor. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486.

f) McCrory has not taught providing system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states. However, Official Notice is taken that prefetching is well known and accepted in the art. Prefetching allows for fetching of instructions/data before the instructions/data are actually needed. Therefore, at the time when they are needed, they are already fetched and present in the system, thereby avoiding any waiting time that might be incurred due to fetching instructions/data as they are needed. In addition, Derrick has taught cache intervention in a multiprocessor system. See column 5, lines 4-14, and note that any L2 cache may intervene and provide the requested data. As is known, cache intervention allows an updated cache to provide data to a requesting device whose cache is not updated. This also prevents the requesting device from having to spend many cycles accessing

main memory for the data. Finally, Derrick has taught an intelligent cache state enhancement. See the abstract and column 3, lines 7-17 and note the implementation of an arbitration scheme for snoop activity. Such a scheme allows for optimized performance and efficient allocation of bandwidth. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to include cache intervention and a cache arbitration scheme which optimize system performance.

19. Referring to claim 2, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory has further taught that the second, heterogenous processor connected to said system bus via said interconnect means, wherein said second, heterogenous processor is comprises more advanced physical and operational characteristics than said first processor, wherein said different physical component parameters include one or more of a higher number of cache levels, larger cache sizes, improved cache hierarchy, cache intervention, and larger number of on-chip processors. See Fig.4 and column 6, lines 28-33, and note that the second processor may be a Pentium-type processor, whereas the first processor may be an 80486-type processor (each processor has different operational characteristics). In addition, looking at Fig.4, the second processor 312 has a larger number of on-chip processors than the first processor 314.

20. Referring to claim 3, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory and Derrick have further taught a cache coherency protocol that supports non-homogenous cache configuration amongst heterogenous processors, said non-homogenous cache configurations including different levels of caches (Derrick, Fig.1), cache states (coherent and incoherent, for

instance), and shared caches among processors. See Derrick, column 1, lines 15-57, and column 3, lines 7-17.

21. Referring to claim 4, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 3. McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has further taught that said interconnect means is coupled to a system bus and comprises a plurality of buses for connecting additional processors to said system bus, said buses comprising a system data bus and base address bus (McCrory, column 6, lines 12-16), a base snoop response bus and extended snoop response bus (Derrick, column 4, lines 45-46, and column 5, lines 16-18). McCrory has further taught a mater processor select bus (column 8, lines 30-50). Note that an interrupt signal (inherently received on a bus) is used to switch processors (to a "master processor") if the current processor cannot execute subsequent code (non-native code). In addition, there would be a bus which is used to send a signal to the processor which is being switched to. Finally, buses like data and address buses clearly include more than one pin.

22. Referring to claim 5, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 4. McCrory has further taught that said master processor select bus includes a first set of pins, each connected to an added processor, wherein when one of said first set of pins is set to an active state, the connected processor operates as a master on the master processor select bus. See column 8, lines 30-50, and note that any of the processors in the system may be switched to in order to execute code native to that processor. Consequently, each processor would be connected to a pin/bus that when active, tells that processor that it will be executing the native code.

23. Referring to claim 6, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 5. Derrick has further taught that:

a) a respective pin is set when a read operation is issued to indicate that the issuing processor is the master processor. See column 5, lines 4-10, and note that a GNT pin is set after a requesting device makes its request (read operation) and the requesting device is granted control.

b) when said read operation is snooped by a second added processor with a cache line in R coherency state, the second added processor drives the extended snoop response bus with shared intervention information and sends a retry response on the base snoop response bus. See column 5, lines 14-18, and note that when another cache has the data requested by the requesting device (in the "R coherency state"), the data is driven onto the extended snoop response bus 126 (Fig. 1) and a response ("retry response") is driven on the base snoop response bus HITM# (Fig.2).

24. Referring to claim 7, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 6. McCrory has further taught that said operational characteristics of each processor connected to the interconnection means include operating frequency, wherein the second processor operates at a higher frequency that said first processor. See column 5, line 66, to column 6, line 8, and note the different operating frequencies.

25. Referring to claim 9, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory and Bacot has further taught a switch that provides direct point-to-point connection between said first processor and later added processors. See Fig.3, column 2, lines 40-47, and column 6, lines 12-20, and

note that processors are added to the system via connector (switch) which allows for point-to-point communication. For instance, in column 6, lines 12-15, McCrory states that processors communicate with one another. One could call the first processor point A and a later added processor point B. Point A would then communicate with point B (point-to-point communication) via the hardware that connects the points. The bus and connectors (switches).

26. Referring to claim 10, McCrory has taught a method for upgrading processing capabilities of a data processing system comprising:

a) providing a plurality of interrupt pins from a system bus on a system planar to allow addition of processors. See the abstract and Fig.3 and note that processors may be added to the system via bus/pins. McCrory has not taught allowing for later addition of other processors. However, Bacot has taught a multiprocessor system in which, when an individual processor breaks or becomes defective, that individual processor is replaced so that the system can return to operating at full capacity. See column 1, lines 57-68. A person of ordinary skill in the art would have recognized that if a processor breaks in McCrory, then the broken processor could be replaced with a functioning processor, thereby allowing symmetric multiprocessing. As a result, in case of individual processor breakage, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory such that a second, heterogenous processor is later added in to the system via interconnection means to allow the system to perform at a higher level.

b) enabling direct connection of a new, heterogenous processor to said system planar via said plurality of interrupt pins, wherein said plurality of interrupt pins provide communication paths

between said heterogenous processor and other processors previously attached to said system planar. See McCrory, column 2, lines 27-47, the abstract, and column 6, lines 12-20.

c) providing support for full backward compatibility by said heterogenous processor when said heterogenous processor comprises more advanced operational characteristics to enable said data processing system to operate as a symmetric multiprocessor system (SMP). See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are more advanced yet backward compatible with 80486. In addition, from the abstract, note that the heterogenous processors allow for symmetric multiprocessing.

d) McCrory has not taught that support includes an enhanced operating system (OS) that supports inter-processing operations between said heterogenous processor and said other processors including cache coherency operations based on a collective memory configuration of the SMP. However, Derrick has taught the concept of employing cache coherency in a multiprocessor system. See column 1, lines 15-27. Cache coherency is employed so that all caches are contain consistent up-to-date data. Otherwise, if a particular cache did not have the most up-to-date data, the processor accessing that cache would be performing operations using incorrect data, which would cause delays in execution. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS to include support for cache coherency.

e) McCrory has not taught that said OS logs operating characteristics and cache topology data of each processor connected to the system bus to calculate a most efficient work allocation among processors. However Cochcroft has taught a system in which process identification codes (operating characteristics) are logged and the number of cache lines used by each process in each

processor (cache topology data) is logged. This data allows for efficient allocation of workload to the processors. See column 1, lines 6-9. As a result, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory's OS log the aforementioned data.

f) McCrory has further taught said interconnection means and said enhanced operating system support backward compatibility between said heterogenous processor and said other processors. See column 6, lines 26-33 and note that Pentiums and 80486s may be used in the system. Pentium chips are backward compatible with 80486.

g) McCrory has not taught providing system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states. However, Official Notice is taken that prefetching is well known and accepted in the art. Prefetching allows for fetching of instructions/data before the instructions/data are actually needed. Therefore, at the time when they are needed, they are already fetched and present in the system, thereby avoiding any waiting time that might be incurred due to fetching instructions/data as they are needed. In addition, Derrick has taught cache intervention in a multiprocessor system. See column 5, lines 4-14, and note that any L2 cache may intervene and provide the requested data. As is known, cache intervention allows an updated cache to provide data to a requesting device whose cache is not updated. This also prevents the requesting device from having to spend many cycles accessing main memory for the data. Finally, Derrick has taught an intelligent cache state enhancement. See the abstract and column 3, lines 7-17 and note the implementation of an arbitration scheme for snoop activity. Such a scheme allows for optimized performance and efficient allocation of bandwidth. As a result, it would have been obvious to one of ordinary skill in the art at the time

of the invention to modify McCrory to include cache intervention and a cache arbitration scheme which optimize system performance.

27. Referring to claim 11, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a method as described in claim 10. Furthermore, claim 11 recites limitations previously recited in claims 4, 5, and 6. Consequently, claim 11 is rejected for the same reasons set forth in the rejections of claims 4, 5, and 6 above.

28. Referring to claim 13, McCrory in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 1. McCrory has further taught a switch that provides direct point-to-point connection between each of said plurality of heterogenous processors. See Fig.3, column 2, lines 40-47, and column 6, lines 12-20, and note that processors are added to the system via connector (switch) which allows for point-to-point communication. For instance, in column 6, lines 12-15, McCrory states that processors communicate with one another. One could call the first processor point A and a later added processor point B. Point A would then communicate with point B (point-to-point communication) via the hardware that connects the points. The bus and connectors (switches). McCrory has not taught connection between each of said plurality of processors and later added processors. However, Bacot has taught a multiprocessor system in which, when an individual processor breaks or becomes defective, that individual processor is replaced so that the system can return to operating at full capacity. See column 1, lines 57-68. A person of ordinary skill in the art would have recognized that if a processor breaks in McCrory, then the broken processor could be replaced with a functioning processor, thereby allowing symmetric multiprocessing. As a result, in case of individual processor breakage, it would have been obvious to one of ordinary

skill in the art at the time of the invention to modify McCrory such that a second, heterogenous processor is later added in to the system via interconnection means to allow the system to perform at a higher level.

29. Referring to claim 15, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 13. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 3 above.

30. Referring to claim 17, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 15. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 4 above.

31. Referring to claim 18, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 17. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 5 above.

32. Referring to claim 19, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 18. Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 6 above.

33. Referring to claim 20, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 19. Furthermore, claim 20 is rejected for the same reasons set forth in the rejection of claim 7 above.

34. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory in view of Bacot in view of Derrick and further in view of Cochcroft, as applied above, and

further in view of MacWilliams et al., U.S. Patent No. 5,228,134 (herein referred to as MacWilliams).

35. Referring to claim 8, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a data processing system as described in claim 3. The aforementioned have not taught that all caches are sectored into widths representing a smallest width cache line that is accessible within the overall system. However, caches are inherently divided into lines having widths, and MacWilliams has taught that conventional parallel cache implementations (plurality of caches) force the line size to be the same. A person of ordinary skill in the art would have recognized that this would allow for a less complex accessing scheme. That is, if all caches are the same size, then accessing is made simple. However, if line sizes were different in each cache, then a more complex scheme would need to be employed. As a result, because MacWilliams has taught that convention systems force cache lines of caches to be the same size, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to include such a feature.

36. Referring to claim 16, McCrory in view of Bacot in view of Derrick and further in view of Cochcroft has taught a multiprocessor system as described in claim 15. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 8 above.

Response To Arguments

37. Applicant's arguments filed on July 27, 2005, have been fully considered but they are not persuasive.

38. Applicant argues on page 10 of the remarks, in substance that:

> "Derrick merely provides a description of a snoop protocol for a SMP that optimizes cache bus bandwidth with no consideration for a later added processor changing the allocation scheme, since Derrick's deals solely with a static system of processors."

39. These arguments are not found persuasive for the following reasons:

a) Applicant appears to be arguing the references individually and one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). For instance, the examiner agrees that Derrick does not teach snooping for an SMP system. Instead, McCrory has taught the SMP system. Derrick was relied on (and combined with McCrory) because of its general teaching of cache coherency. Regardless of whether a static system or dynamic system exists, cache coherency is an essential feature; otherwise the caches of the multiple processors will contain invalid data. Therefore, it would have been obvious to one of ordinary skill in the art to apply the general teaching of cache coherency, as taught by Derrick, to McCrory.

40. Applicant argues on page 11 of the remarks, in substance that:

> "With respect to Cochcroft, it appears that examiner has either mischaracterized what is provided by Cochcroft or fails to comprehend what is being taught by applicants' claims. Examiner writes that Cochcroft's recitation of process identification code suggests applicants' claimed "operating characteristics." This analysis is clearly incorrect. Operating characteristics specifically refers to characteristics/parameters such as different processing speeds (frequency), different IC design, different cache topologies (sizes, levels, etc.)."

41. These arguments are not found persuasive for the following reasons:

a) The examiner asserts that applicant is arguing features which are not found in the claims. Specifically, claim 7 further defines "said operational characteristics". Claim 1, which is ultimately the parent of claim 7, states that a first processor includes "operational characteristics" and also states that an OS logs "operating characteristics". Consequently, the characteristics that

are logged by the OS have nothing to do with the characteristics of claim 7. A similar argument applies for claims 12 and 20.

42. Applicant argues on page 11 of the remarks, in substance that:

> "Finally, Bacot provides a description of replacing a defective/bad processor within a system (when the processor breaks). Bacot most likely completes the replacement with a similar processor. No enhanced OS is required or other features for later adding a heterogenous processor and providing OS and other support for that newly added processor in addition to all other existing processors. Bacot does not add another processor without first removing an existing processor because Bacot's system has no expansion mechanism for adding additional processors and Bacot never contemplates adding more processors or providing OS support for more processors or even adding a heterogenous processor."

43. These arguments are not found persuasive for the following reasons:

a) Even if applicant is correct in saying that Bacot replaces a broken processor with a processor of the same type, this replacement processor is still heterogenous with respect to a first processor in the system. For instance, looking at Fig.3 of McCrory, if processor 314 breaks, a new processor 314 may be added and the new processor (being of FAM2) is still heterogenous with respect to the other processors. Applicant's claim does not state that a processor may not be removed (or that adding a processor is not adding to replace a broken processor). In addition, all of the enhanced OS support necessary to control processors of McCrory (Fig.3) would exist to control processors before and after replacement. And, an enhanced OS has been shown to exist as claimed by applicant for reasons in the rejections above.

Conclusion

44. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
September 12, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100